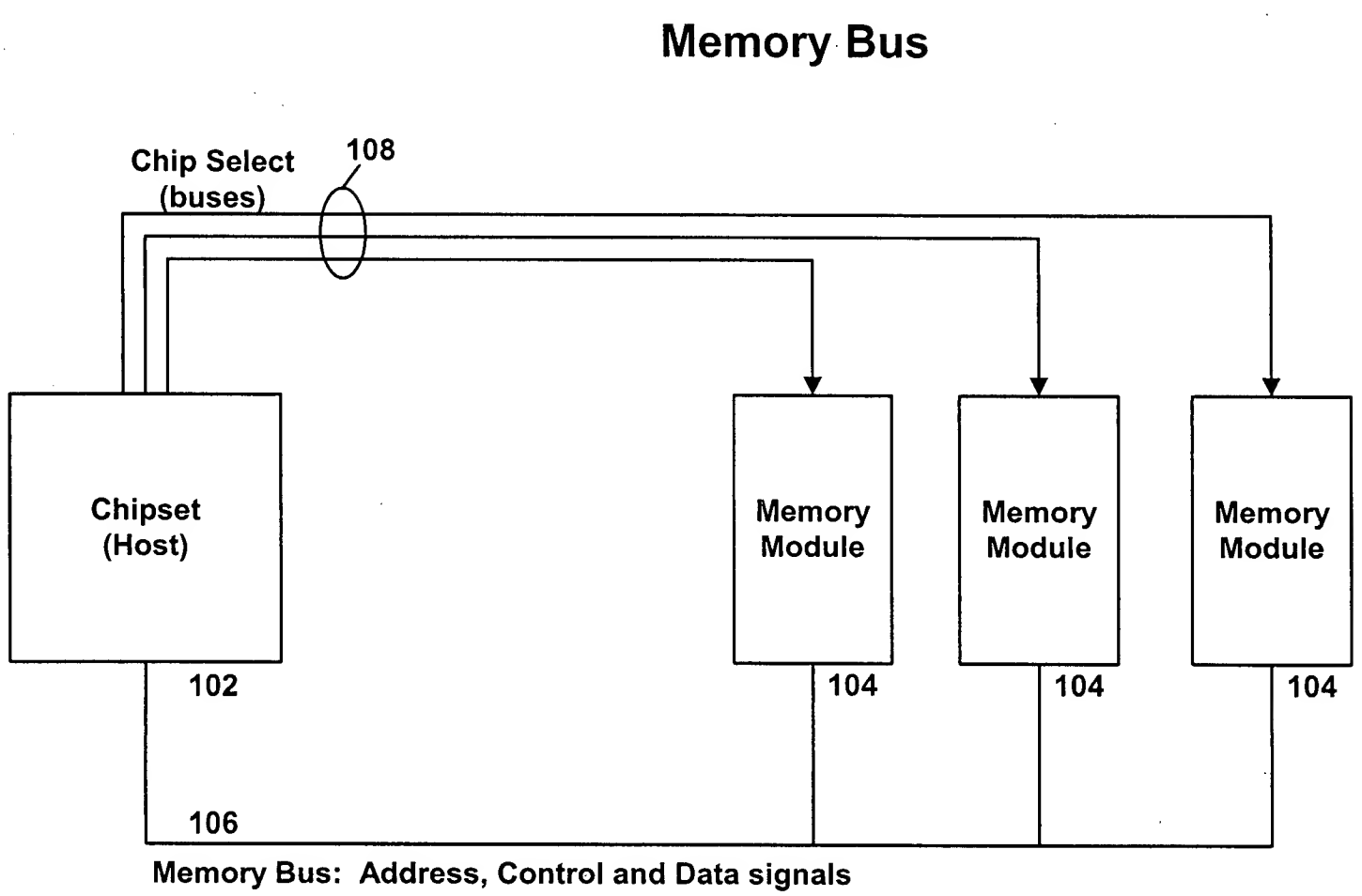

Figure 1
(Prior Art)

Memory Bus Peripheral (FPGA) Operation

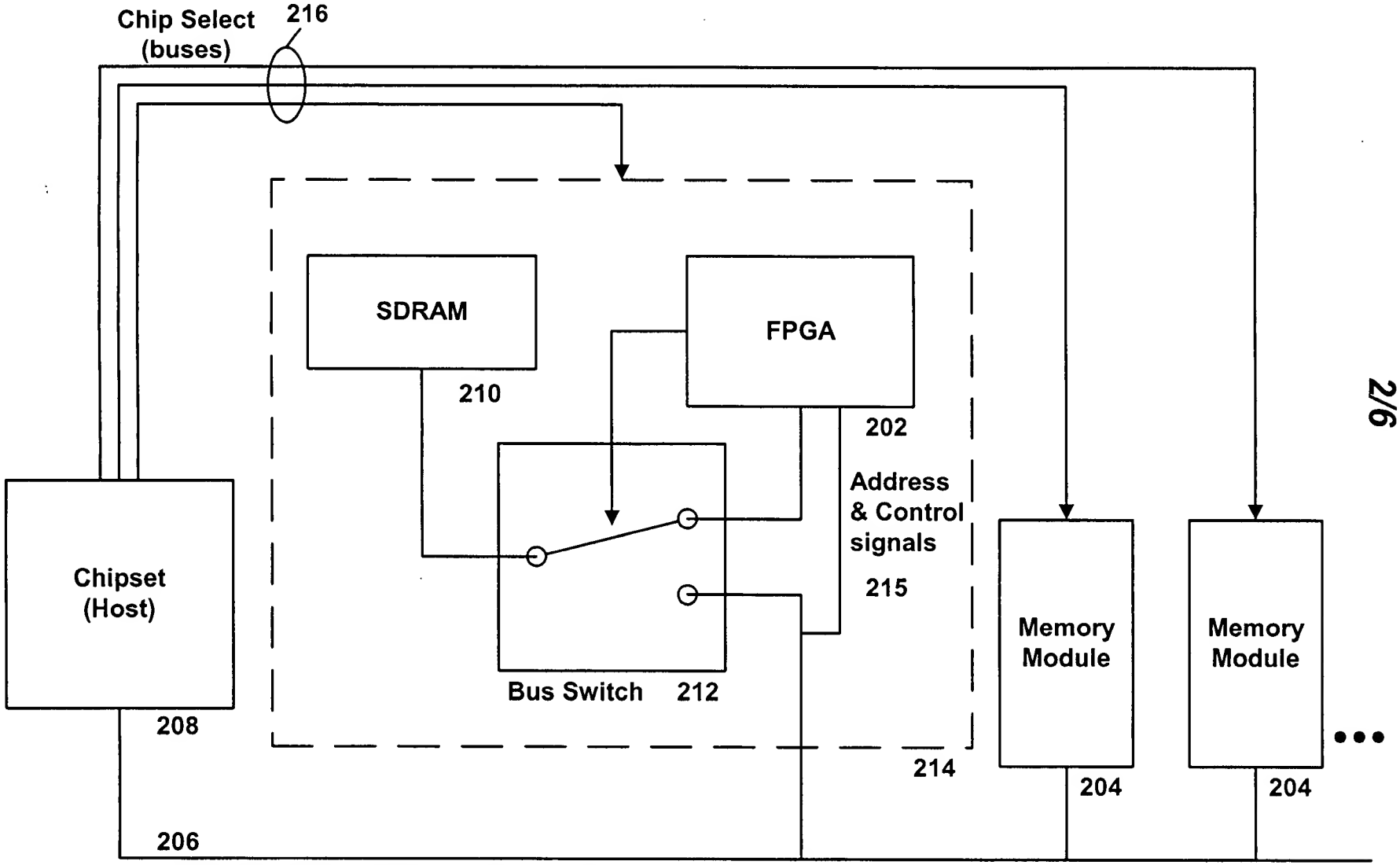

Figure 2

Operational Flowchart

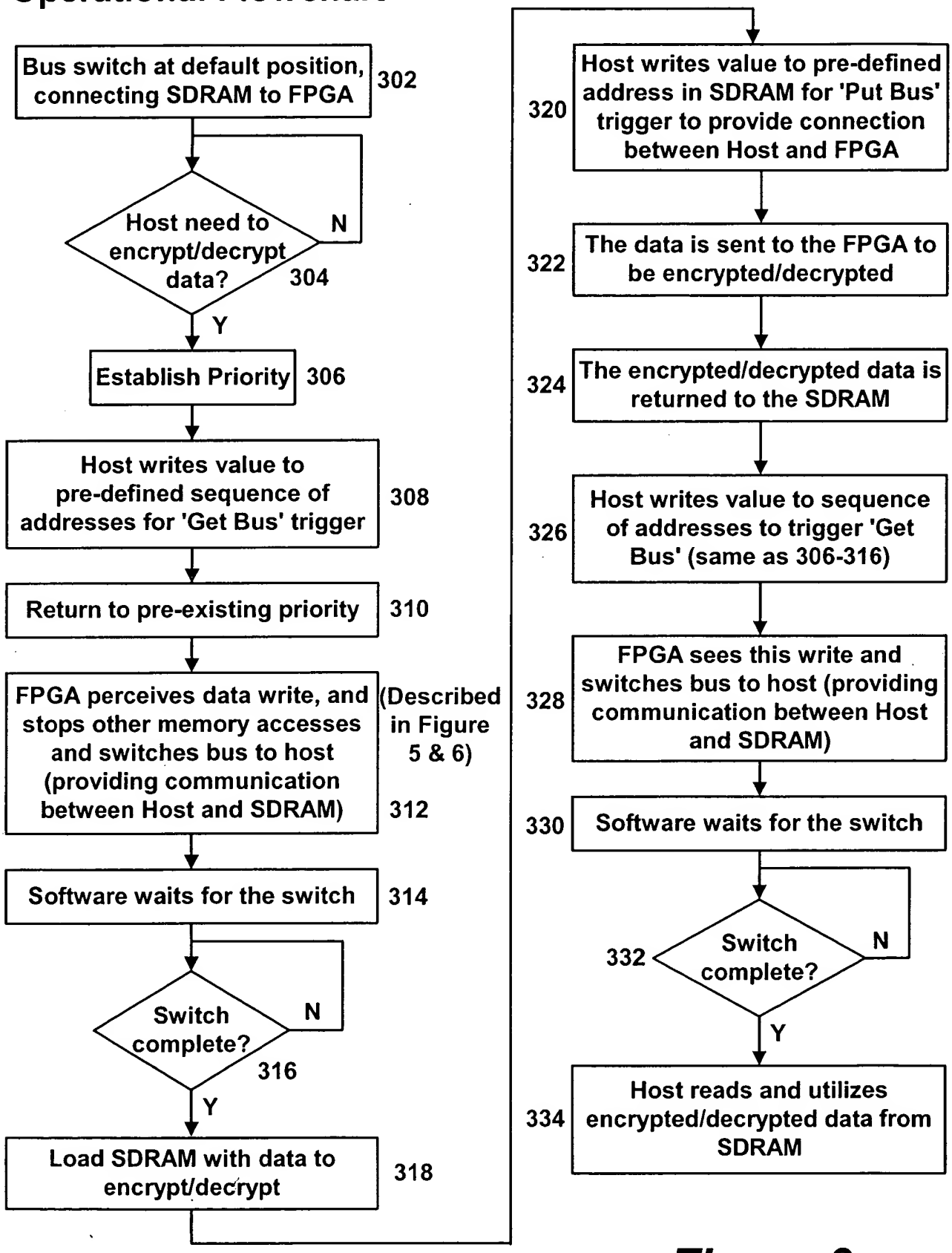

Figure 3

Example Memory Module Trigger Address Locations

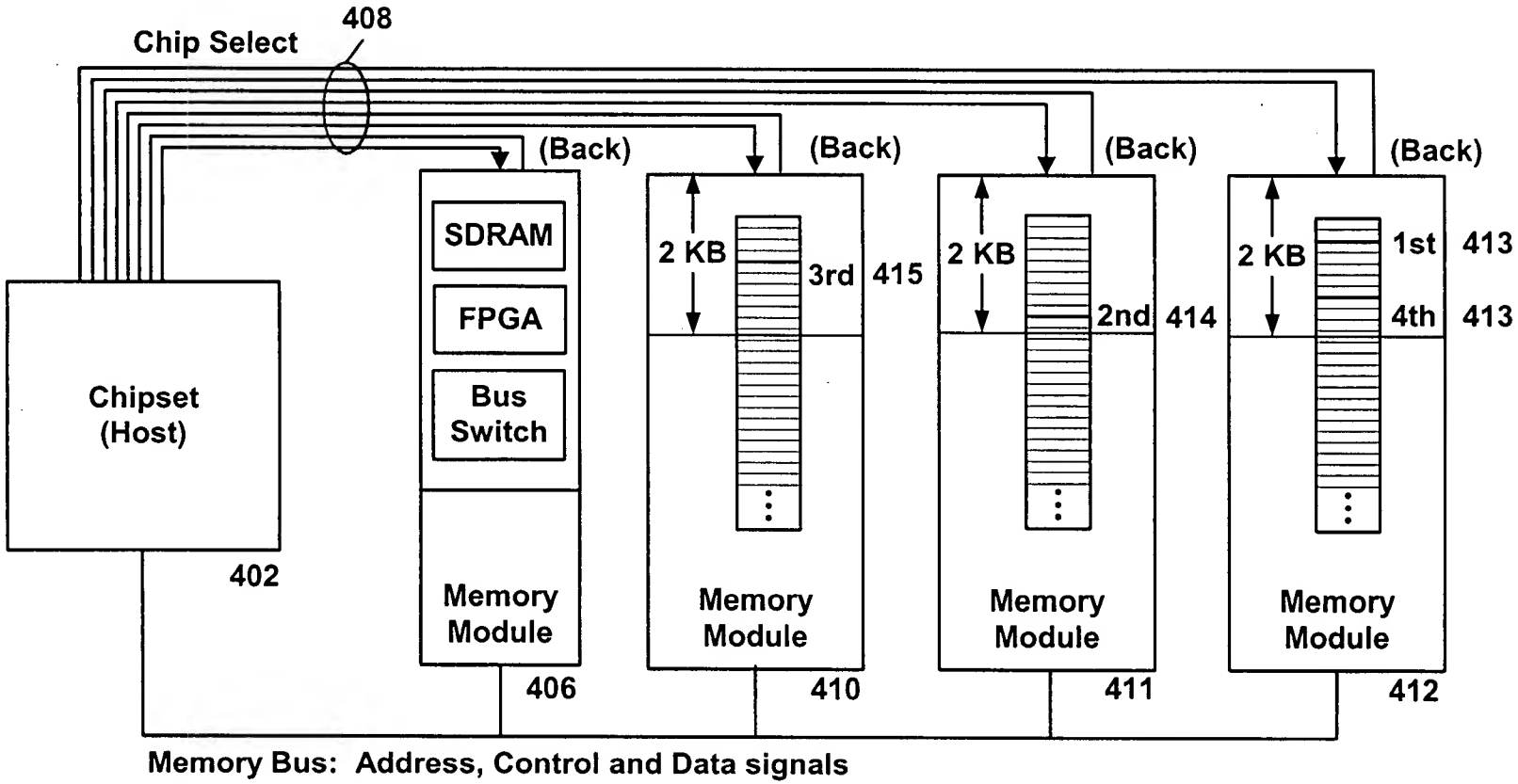

Figure 4

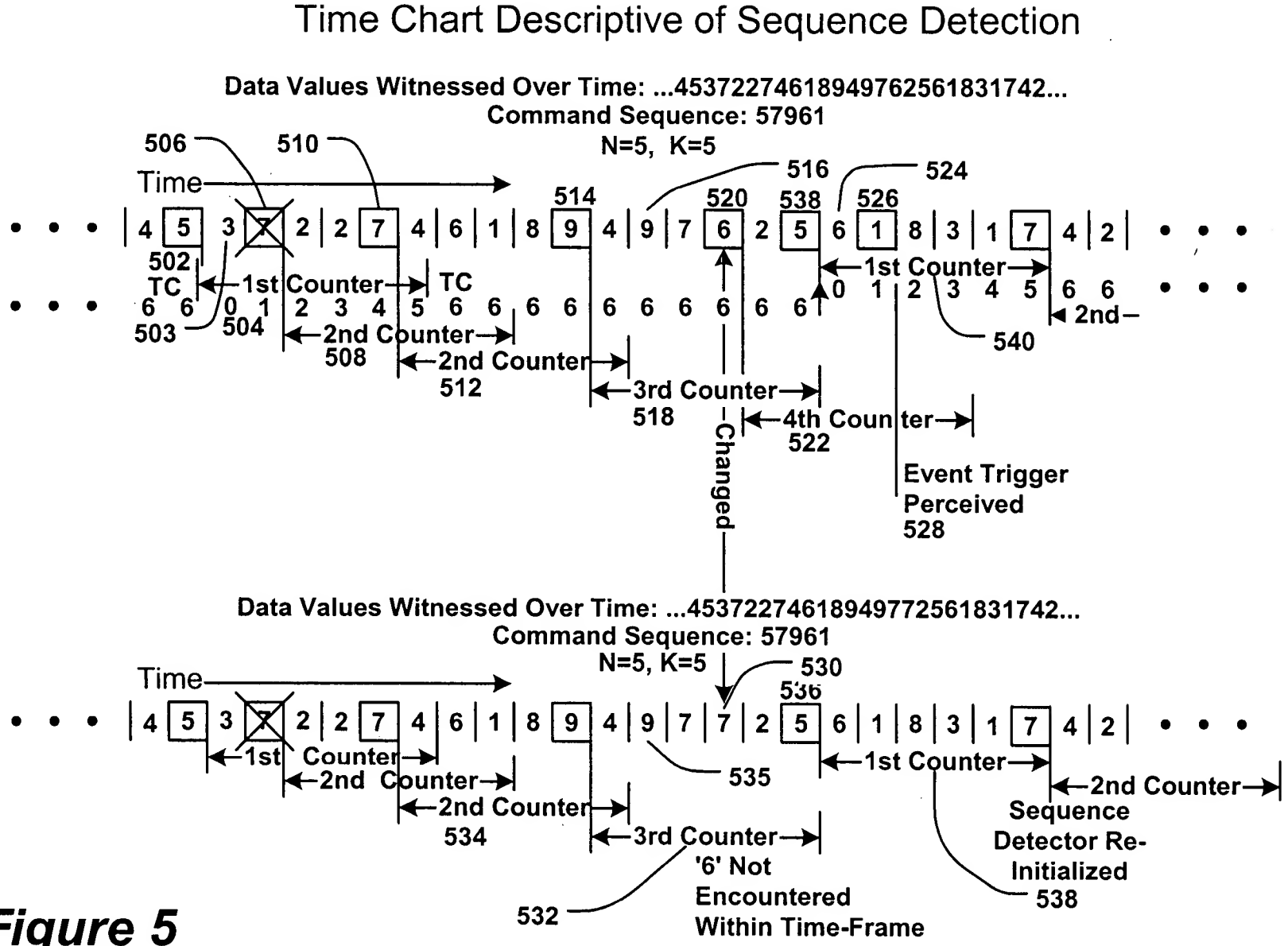

Figure 5

General Schematic of Data Value Sequence Detector

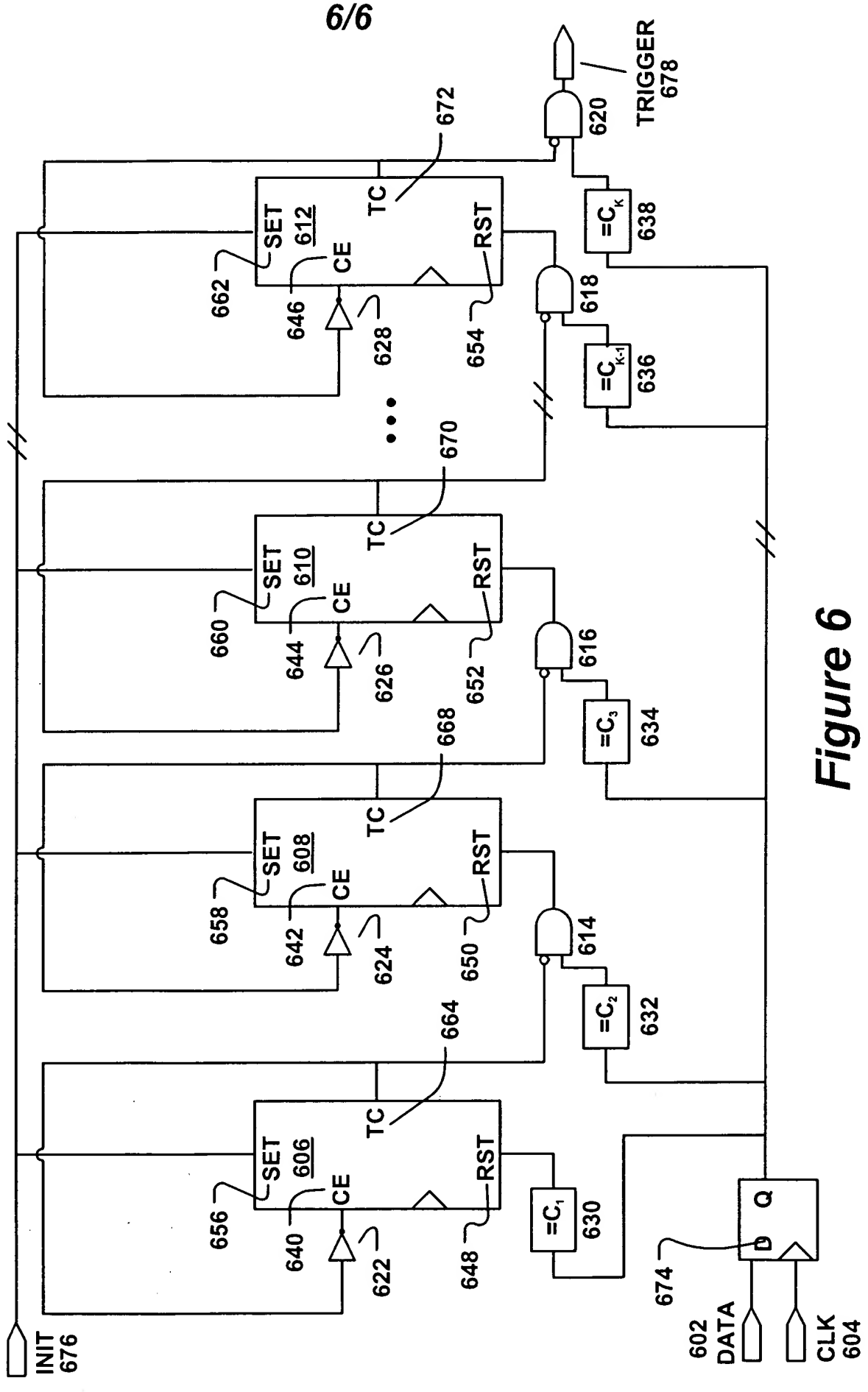

Figure 6